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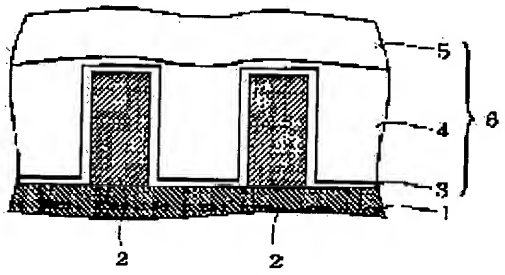
(71)Applicant : **MITSUBISHI ELECTRIC CORP**
(72)Inventor : **MATSUURA MASAZUMI**

(54) SEMICONDUCTOR DEVICE, METHOD AND APPARATUS FOR MANUFACTURE THEREOF AND METHOD OF FORMING INSULATION FILM OF SEMICONDUCTOR DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To lower the dielectric const. and improve the burying characteristic by forming an insulation film by the chemical vapor deposition using a mixed gas of a silane-based gas and hydrogen peroxide and a mixed gas of silane and hydrogen peroxide.
SOLUTION: On an Si substrate 1 an Al wiring 2 is laid, a lower layer plasma oxide film 3 is formed on the surface of the substrate 1 and Al wiring 2, an Si oxide film 4 is formed on the film 3 by the chemical vapor deposition using a mixed gas of monomethyl silane which is a silane type gas contg. Si atoms coupled with hydrocarbon groups, silane and hydrogen peroxide water, and an upper layer plasma oxide film 5 is formed on the oxide film 4 to obtain a flat layer insulation film 6. This lowers the dielectric cost. And improves the burying characteristic.



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* NOTICES *

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The insulator layer formation method of a semiconductor device which forms an insulator layer by the chemical-vapor-deposition method using the silane system gas and the silane containing the silicon atom combined with the silane system gas, the mixed gas of hydrogen peroxide solution, or the aforementioned hydrocarbon group containing the silicon atom which is the insulator layer formation method of a semiconductor device, and was combined with the hydrocarbon group, and the mixed gas of hydrogen peroxide solution.
[Claim 2] The aforementioned hydrocarbon group is the insulator layer formation method of a semiconductor device according to claim 1 characterized by being an alkyl group.
[Claim 3] The aforementioned alkyl group is the insulator layer formation method of a semiconductor device according to claim 2 characterized by being a methyl group, a dimethyl machine, or a trimethyl basis.
[Claim 4] The aforementioned alkyl group is the insulator layer formation method of a semiconductor device according to claim 2 characterized by being an ethyl group, a diethyl machine, or a triethyl machine.
[Claim 5] The aforementioned hydrocarbon group is the insulator layer formation method of a semiconductor device according to claim 1 characterized by being a vinyl group.
[Claim 6] The range of the temperature at the time of formation of the aforementioned insulator layer the range of the pressure at the time of formation of -10-60 degrees C and the aforementioned insulator layer 400 - 2000mTorr, More ranges of the quantity of gas flow of the silane system gas containing the silicon atom which combined the range of the quantity of gas flow of the aforementioned silane with 0 - 120sccm and the aforementioned hydrocarbon group than 0sccm 120 or less sccms, The range of the quantity of gas flow of the aforementioned hydrogen peroxide solution is the insulator layer formation method of a semiconductor device according to claim 1 to 5 characterized by being 0.35 - 0.85 g/min.
[Claim 7] It is the semiconductor device which is equipped with the layer insulation film formed between a semiconductor substrate, the multilayer metal wiring formed on the aforementioned semiconductor substrate, and the aforementioned multilayer metal wiring on the aforementioned semiconductor substrate, and is characterized by the aforementioned layer insulation film containing the silicon atom combined with the hydrocarbon group.
[Claim 8] The aforementioned layer insulation film is a semiconductor device according to claim 7 characterized by being formed by the insulator layer formation method of a semiconductor device according to claim 1 to 6.
[Claim 9] It is the manufacture method of a semiconductor device which is equipped with the 1st process for which a semiconductor substrate is prepared, the 2nd process which forms metal wiring on the aforementioned semiconductor substrate, and the 3rd process which forms a wrap insulator layer for the aforementioned metal wiring on the aforementioned semiconductor substrate, and is characterized by forming the aforementioned insulator layer by the insulator layer formation method of a semiconductor device according to claim 1 to 6.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] Especially this invention relates to the formation method of a layer insulation film of filling between metal wiring, about a semiconductor device, its manufacture method, and its insulator layer formation method.
[0002]
[Description of the Prior Art] Drawing showing the typical manufacturing process of the layer insulation film in the conventional semiconductor device is shown in drawing 15 - drawing 17 .
[0003] In drawing 15 - drawing 17 , each reference mark shows the following. The element which 1p does not illustrate, the silicon substrate in which the insulating layer is formed, the silicon oxide in which a lower layer plasma oxidation film and 4p were formed [2p] for aluminum wiring and 3p by the plasma CVD method using SiH4 and the mixed gas of H2O2, and 5p are layer insulation films with which the upper plasma oxidation film and 6p consist of plasma oxidation film 3p, silicon-oxide 4p, and plasma oxidation film 5p.
[0004] Next, detailed explanation of the manufacturing process in which layer insulation film 6p is formed is given.
[0005] As shown in drawing 15 , aluminum wiring 2p is formed on silicon-substrate 1p, and as the front face of silicon-substrate 1p and aluminum wiring 2p is worn, plasma oxidation film 3p which is a lower layer is formed.
[0006] Next, as shown in drawing 16 , silicon-oxide 4p is formed by CVD using SiH4 and the mixed gas of H2O2. In addition, on the whole, silicon-oxide 4p has covered lower layer plasma oxidation film 3p.
[0007] If the upper plasma oxidation film 5p is finally formed so that the whole silicon-oxide 4p may be covered as shown in drawing 17 , the semiconductor device which has flat layer insulation film 6p will be obtained.
[0008] Silicon-oxide 4p in this case is generated by the following reaction formulas.
[0009] First, oxidation reaction of SiH four H2O2 shown below generates a silanol (Si4 (OH)).
[0010]
[Formula 1]

$$SiH_4 + 2H_2O_2 \rightarrow Si(OH)_4 + 2H_2$$

[0011]
[Formula 2]

$$SiH_4 + 3H_2O_2 \rightarrow Si(OH)_4 + 2H_2O + H_2$$

[0012]
[Formula 3]

$$SiH_4 + 4H_2O_2 \rightarrow Si(OH)_4 + 4H_2O$$

[0013] Next, the formed silanol is that dehydration polymerization reaction occurs with the hydrolysis or heat energy shown below, and generates a silicon oxide (SiO2).
[0014]
[Formula 4]

$$n\,Si(OH)_4 \rightarrow n\,SiO_2 + 2n\,H_2O$$

[0015] A silicon oxide will be formed when such a chemical reaction occurs on silicon-substrate 1p.
[0016] At this time, the molecular structure of formed silicon-oxide 4p consists of only Si-O combination and Si-OH combination, as shown in drawing 18 . Moreover, Si atoms are combined through O atom.
[0017]
[Problem(s) to be Solved by the Invention] Since the conventional semiconductor device is constituted as mentioned above, it has connoted the following troubles.
[0018] That is, when describing briefly the Prior art mentioned above, the layer insulation film in a semiconductor device formed the silicon oxide by the CVD (Chemical Vapor Deposition) method using mixed gas with a silicon compound (SiH4), for example, a silane, and a hydrogen peroxide (H2O2). This silicon oxide can embed between very detailed wiring of 0.25

micrometers or less. furthermore, from excelling in a fluidity and this showing self-planation As the flattening technique of the next-generation layer insulation film which replaces the SOG (Spin on glass) method currently used from the former It is observed (). [NOVEL SELF-PLANARIZING CVD OXIDE FOR INTERLAYER DIELECTRIC APPLICATIONS"(117 - 120 pages of Technical digestof IEDM'94)] And it indicates to "PLANARISATION FOR SUB-MICRON DEVICES UTILIZINGA NEW CHEMISTRY" (94 - 100 pages of Proceedings of DUMIC conference'95).

[0019] However, the specific inductive capacity of the silicon oxide (** 4) generated from the silanol (** 1 --izing 3) is 4.0-5.0. The problem of the signal delay by wiring resulting from the parasitic capacitance of a layer insulation film is becoming serious with detailed-izing of a device in recent years. For this reason, in the layer insulation film formed in a semiconductor device, it is becoming an important problem to reduce the parasitic capacitance. It is a problem of the utmost importance to decrease the parasitic capacitance during the metal wiring with which between metal wiring became detailed with 0.3 micrometers or less especially. For that purpose, the layer insulation film excellent in reduction, the embedding nature, and the flattening property of specific inductive capacity is called for.

[0020] This invention is made in order to cancel the above troubles, and it is growing up a silane, silane system gas, the mixed gas of hydrogen peroxide solution, or silane system gas and the mixed gas of hydrogen peroxide solution as a silicon oxide by CVD, and it embeds, and also has a performance and a self-flattening property and it aims at offering the outstanding semiconductor device with which specific inductive capacity falls further, its manufacture method, and its insulator layer formation method.

[0021]

[Means for Solving the Problem] The insulator layer formation method of the semiconductor device concerning the 1st invention forms an insulator layer by the chemical-vapor-deposition method using the silane system gas and the silane containing the silicon atom combined with the silane system gas, the mixed gas of hydrogen peroxide solution, or the aforementioned hydrocarbon group containing the silicon atom combined with the hydrocarbon group, and the mixed gas of hydrogen peroxide solution.

[0022] The insulator layer formation method of the semiconductor device concerning the 2nd invention is the insulator layer formation method of the semiconductor device the 1st invention, and it is characterized by the aforementioned hydrocarbon group being an alkyl group.

[0023] The insulator layer formation method of the semiconductor device concerning the 3rd invention is the insulator layer formation method of the semiconductor device the 2nd invention, and it is characterized by the aforementioned alkyl group being a methyl group, a dimethyl machine, or a trimethyl basis.

[0024] The insulator layer formation method of the semiconductor device concerning the 4th invention is the insulator layer formation method of the semiconductor device the 2nd invention, and it is characterized by the aforementioned alkyl group being an ethyl group, a diethyl machine, or a triethyl machine.

[0025] The insulator layer formation method of the semiconductor device concerning the 5th invention is the insulator layer formation method of the semiconductor device the 1st invention, and it is characterized by the aforementioned hydrocarbon group being a vinyl group.

[0026] The insulator layer formation method of the semiconductor device concerning the 6th invention It is the insulator layer formation method of a semiconductor device given in either the 1st invention or the 5th invention. The range of the temperature at the time of formation of the aforementioned insulator layer the range of the pressure at the time of formation of -10-60 degrees C and the aforementioned insulator layer 400 - 2000mTorr, More ranges of the quantity of gas flow of the silane system gas containing the silicon atom which combined the range of the quantity of gas flow of the aforementioned silane with 0 - 120sccm and the aforementioned hydrocarbon group than 0sccm 120 or less sccms, It is characterized by the range of the quantity of gas flow of the aforementioned hydrogen peroxide solution being 0.35 - 0.85 g/min.

[0027] The semiconductor device of the 7th invention is equipped with the layer insulation film formed between a semiconductor substrate, the multilayer metal wiring formed on the aforementioned semiconductor substrate, and the aforementioned multilayer metal wiring on the aforementioned semiconductor substrate, and it is characterized by the aforementioned layer insulation film containing the silicon atom combined with the hydrocarbon group.

[0028] The semiconductor device of invention of the octavus is a semiconductor device of the 7th invention, and it is characterized by forming the aforementioned layer insulation film in either the 1st invention or the 6th invention by the insulator layer formation method of the semiconductor device a publication.

[0029] The manufacture method of the semiconductor device the 9th invention is equipped with the 1st process for which a semiconductor substrate is prepared, the 2nd process which forms metal wiring on the aforementioned semiconductor substrate, and the 3rd process which forms a wrap insulator layer for the aforementioned metal wiring on the aforementioned semiconductor substrate, and the aforementioned insulator layer is characterized by to be formed in either the 1st invention or the 6th invention by the insulator layer formation method of the semiconductor device a publication.

[0030]

[Embodiments of the Invention]

(Gestalt 1 of operation) The gestalt 1 of implementation of this invention is hereafter explained based on drawing 1 - drawing 5 .

[0031] Drawing 1 - drawing 3 are the cross sections showing typically the manufacturing process of the semiconductor device in the gestalt 1 of operation. Drawing 4 is drawing showing typically the molecular structure of the silicon oxide in the gestalt

1 of operation. drawing 5 is a graph showing the result of the measurement which is each specific inductive capacity of the silicon oxide of a Prior art, and the silicon oxide in the gestalt 1 of operation

[0032] First, in drawing 1 , the aluminum wiring 2 (metal wiring) is arranged on the silicon substrate 1 (semiconductor substrate). The element and insulating layer which are not illustrated are formed in this silicon substrate 1. On a silicon substrate 1 and the front face of the aluminum wiring 2, the lower layer plasma oxidation film 3 is formed. In addition, this plasma oxidation film 3 is formed by the plasma CVD method. As for the general formation conditions by the plasma CVD method of the plasma oxidation film 3 at this time, formation temperature forms [300degreeC and the pressure] by 750mTorr(s) and RF power using SiH4 and a nitrous oxide (N2O) for 500W and material gas. The thickness of the plasma oxidation film 3 is 1000A. In this case, you may form the plasma oxidation film 3 by the plasma CVD method, using formation temperature 400degreeC, pressure 5Torr, and RF power as 500W as general formation conditions, using TEOS (Tetraethoxysilane) and oxygen as material gas.

[0033] Next, after the end of the manufacturing process of drawing 1 forms a silicon oxide 4 (HMO:Hydrogen peroxide and Methylsilane based CVD Oxide) by the plasma CVD method (chemical-vapor-deposition method) on the lower layer plasma oxidation film 3 using the monomethyl silane (SiH3CH3) which is one kind of the gas of the silane system containing the silicon atom combined with the hydrocarbon group, a silane (SiH4), and the mixed gas of hydrogen peroxide solution (H2O2), as shown in drawing 2 . Thus, the silicon oxide 4 is filling between the aluminum wiring 2 completely so that the aluminum wiring 2 may be covered.

[0034] This monomethyl silane, a silane, and the mixed gas of hydrogen peroxide solution cause a chemical reaction as shown below.

[0035] First, SiCH3(OH)3 are generated by oxidation reaction of SiH3CH 3 andH2O2 shown below (** 5). simultaneously, the Prior art showed -- Si (OH)4 is also generated by the chemical reaction of SiH 4 andH2O2 (** 1, 2, and 3)

[0036]

[Formula 5]

$$2\,SiH_3(CH_3) + 3\,H_2O_2 \rightarrow 2\,Si(CH_3)(OH)_3$$

[0037] Next, SiCH3(OH)3 formed are that the dehydration condensation reaction by the hydrolysis or heat energy shown below occurs, and Si(CH3) O1.5 are generated (** 6). SiO2 is generated because the dehydration condensation reaction also according [Si (OH)4] to hydrolysis or heat energy occurs (** 4).

[0038]

[Formula 6]

$$2n\,Si(CH_3)(OH)_3 \rightarrow 2n\,Si(CH_3)O_{1.5} + 3n\,H_2O$$

[0039] this intermediate fields of SiCH3 (OH)3 and Si (OH)4 or Si (CH3) mentioned above -- the HMO film 4 as shown in drawing 2 is formed of the reaction of the end products of O1.5 and SiO2

[0040] in addition, since this HMO film 4 has the fluidity which was excellent like Si (OH)4 of a Prior art, the embedding of it which it is between very detailed aluminum wiring becomes possible

[0041] Finally, after the end of the manufacturing process of drawing 2 , as shown in drawing 3 , it is forming the upper plasma oxidation film 5 on a silicon oxide 4, and the flat layer insulation film 6 is obtained. In addition, the formation conditions of this plasma oxidation film 5 are the same formation conditions as the lower layer plasma oxidation film 3. It is a book though it is different conditions.

[0042] Moreover, aluminum wiring of the two-layer eye which is not illustrated is formed in the upper layer of this plasma oxidation film 5, and a plasma oxidation film, a silicon oxide, and a plasma oxidation film are formed in it like the case where it is the 1st layer. At this time, it is completely buried by the silicon oxide between aluminum wiring of a two-layer eye, and it becomes possible to attain flattening. in addition, the connection which connects the lower layer aluminum wiring 2 and aluminum wiring of the upper layer which is not illustrated -- a hole is formed Then, the 3rd layer, and the 4th layer and aluminum wiring which is not illustrated if needed are formed, between aluminum wiring is completely filled by the silicon oxide in the semiconductor device which has multilayer-interconnection structure, and flattening of a semiconductor device can plan.

[0043] Next, the formation conditions of a silicon oxide 4 (HMO film) mentioned above are described.

[0044] As the formation method of the gestalt 1 this operation, hydrogen peroxide solution (H2O2) and a silane (SiH4) are added in alkyl silane (SiHx 4-x (CH3)) gas in the manufacturing process of the silicon oxide 4 mentioned above. The alkyl silane used with the gestalt 1 of this operation is a monomethyl silane (SiH3CH3), and formation temperature formation conditions - The quantity of gas flow of 0-120 (sccm), and SiH3CH3 has more quantities of gas flow of 400-2000 (mTorr), and SiH4 than 0 (sccm), and 10-60 (degreeC), and a formation pressure take below 120 (sccm) for the quantity of gas flow of H2O2 carrying out by 0.35 - 0.85 g/min.

[0045] Under the present circumstances, the quantity of gas flow which doubled SiH3CH3 with SiH4 is 120 (sccm) desirably. That is, for example, when SiH4 is set to 50 (sccm), SiH3CH3 is set to 70 (sccm). Moreover, when the quantity of gas flow of SiH3CH3 will increase when decreasing the quantity of gas flow of SiH4, and another side and the capacity of SiH4 are made to increase, the quantity of gas flow of SiH3CH3 will decrease. Under the conditions of SiH4 in this case, and the quantity of gas flow of SiH3CH3 (the quantity of gas flow of SiH4 and SiH3CH3 is not 0 (sccm)), as shown in drawing 4 , a silicon oxide

will have the molecular structure of Si-O combination, Si-CH3 combination, and Si-OH combination. In addition, through O atom, Si atom is combined so that it may become the skeleton of the whole silicon-oxide molecule.
[0046] If the molecular structure of a silicon oxide is explained in detail here and the silicon oxide (drawing 4) of the gestalt 1 of this operation will be compared with the silicon oxide (drawing 18) of a Prior art, in the silicon oxide of a Prior art, Si-CH3 combination which did not exist exists as the molecular structure of a silicon oxide. From this, Si atom will escape from the place where Si atom existed by the Prior art, micro space will come to exist in the marks, and the density of the whole silicon oxide will fall. Consequently, compared with a Prior art, as for the silicon oxide of the gestalt 1 of this operation, specific inductive capacity will fall because density falls.
[0047] the silicon oxides according to the gestalt 1 of this operation to the specific inductive capacity of the silicon oxide shown in drawing 5 which it is as a result of the experiment of the gestalt 1 of this operation according [each specific inductive capacity of the gestalt 1 of a Prior art and this operation] to a Prior art like being 4.5 are 3.3-3.4
[0048] As explained above, compared with the silicon oxide of a Prior art, low dielectric constant-ization of the specific inductive capacity of the silicon oxide by the gestalt 1 of this operation is attained.
[0049] Thus, using the mixed gas of a monomethyl silane, a silane, and hydrogen peroxide solution, even if a monomethyl silane and hydrogen peroxide solution are used for the silicon oxide by invention of the gestalt 1 of this operation, it can acquire the effect of the reduction in a dielectric constant same as a result. Moreover, embedding during metal wiring is made possible and the property of outstanding self-flattening is also held.
[0050] In addition, with the gestalt 1 of this operation, although the HMO film 4 was formed on the lower layer plasma oxidation film 3, you may form on the direct aluminum wiring 2, without forming the plasma oxidation film 3.
[0051] (Gestalt 2 of operation) Although the gestalt 1 of operation showed above the example which used the monomethyl silane (SiH3CH3) as an alkyl silane, the same effect is done so even if it uses dimethylsilane (SiH2(CH3) 2) and a trimethyl silane (SiH3 (CH3)).
[0052] Hereafter, the gestalt 2 of implementation of this invention is explained based on drawing.
[0053] Drawing 6 is drawing showing typically the molecular structure at the time of forming a silicon oxide using dimethylsilane. Drawing 7 is drawing showing typically the molecular structure at the time of forming a silicon oxide using a trimethyl silane. Drawing 8 is a graph showing the specific inductive capacity of the silicon oxide of a Prior art, and the silicon oxide of the gestalt 2 of this operation.
[0054] The silicon oxide of the gestalt 2 of this operation manufactures a semiconductor device by the manufacture method shown by drawing 1 - drawing 3 like the HMO film 4 of the gestalt 1 of operation. It only differs that the gas used as the raw material used with the gestalt 1 of operation changed to dimethylsilane or the trimethyl silane from the monomethyl silane. The conditions (formation temperature, a formation pressure, quantity of gas flow, etc.) which form a silicon oxide in the gestalt 2 of this operation are the completely same conditions as the gestalt 1 of operation, and generate by the plasma CVD method. Moreover, the same is said of the point which adds only hydrogen peroxide solution, a silane, or hydrogen peroxide solution to dimethylsilane or a trimethyl silane, is made to cause the chemical reaction of mixed gas, and generates a silicon oxide.
[0055] Hereafter, the reaction formula of the gestalt 2 of this operation is explained.
[0056] Si(CH3)2(OH)2 are generated because the oxidation reaction which shows first below the dimethylsilane used with the gestalt 2 of this operation occurs (** 7).
[0057]
[Formula 7]

$$SiH_2(CH_3)_2 + 2H_2O_2 \rightarrow Si(CH_3)_2(OH)_2$$

[0058] Next, Si (CH3) 2O2 is generated because a dehydration condensation reaction occurs [Si(CH3)2(OH)2 generated] (** 8).
[0059]
[Formula 8]

$$n\,Si(CH_3)_2(OH)_2 \rightarrow n\,Si(CH_3)_2O_2 + n\,H_2O$$

[0060] Moreover, a chemical reaction as well as [a silane] the gestalt 1 of operation occurs, and intermediate field (OH) Si 4 and an end product SiO2 are generated (** 1, 2, 3, and 4). Intermediate field (CH3) (OH) Si 2 The silicon oxide 4 of drawing 3 is created by the reaction of 2 and Si(OH)4 comrades or an end product (CH3) Si 2O2, and SiO2 comrades.
[0061] On the other hand, a trimethyl silane is that oxidation reaction (** 1, 2, and 3) and a dehydration condensation reaction (** 4) occur also in a silane while the chemical reaction of oxidation reaction (** 9) and a dehydration condensation reaction (** 10) shown below occurs, and the silicon oxide 4 of drawing 3 is created.
[0062]
[Formula 9]

$$SiH(CH_3)_3 + H_2O_2 \rightarrow Si(CH_3)_3(OH)$$

[0063]
[Formula 10]

$$n\,Si(CH_3)_3(OH) \rightarrow n\,Si(CH_3)_3O + n\,H_2O$$

[0064] In addition, since the silicon oxide 4 of drawing 3 generated from dimethylsilane and the trimethyl silane holds the outstanding fluidity, it makes possible embedding during aluminum wiring of microscopic **.
[0065] The molecular structure of the silicon oxide of the gestalt 2 of this operation at the time of adding hydrogen peroxide solution and a silane to dimethylsilane or a trimethyl silane consists of Si-O combination, Si-OH combination, and Si-CH3 combination, as shown in drawing 6 and drawing 7 . In Si atom, two or the thing combined three also has per [CH / three] Si atom. Thus, Si atom has escaped from the place where Si atom existed in the Prior art by the ratio like the HMO film 4 (drawing 4) of the gestalt 1 of operation. For this reason, space will come to exist in the marks from which it escaped, and the density of the whole silicon oxide will fall to them. Consequently, into the molecule of the silicon oxide of the gestalt 2 of this operation, the density of a silicon oxide will fall like the HMO film of the gestalt 1 of operation.
[0066] Thus, it becomes possible to aim at decline in specific inductive capacity because the density within the molecular structure of a silicon oxide falls. Moreover, the embedding property which could fill between the aluminum wiring 2 by the silicon oxide, and was excellent is realizable. Moreover, it also becomes possible to realize the outstanding self-flattening property.
[0067] as shown in drawing 8 which it is as a result of the experiment of the gestalt 2 of this operation, the silicon oxides by the gestalt 2 which is this operation to each specific inductive capacity of the silicon oxide of a Prior art and the silicon oxide of the gestalt 2 of this operation being the specific inductive capacity 4.5 of the silicon oxide by the Prior art are 3.3-3.4
[0068] As explained above, the specific inductive capacity of the silicon oxide by the gestalt 2 of this operation becomes possible [aiming at decline in specific inductive capacity] compared with the silicon oxide of a Prior art.
[0069] Thus, the silicon oxide by invention of the gestalt 2 of this operation can acquire the effect of the reduction in a dielectric constant using the mixed gas of dimethylsilane or a trimethyl silane, a silane, the mixed gas of hydrogen peroxide solution, dimethylsilane or a trimethyl silane, and hydrogen peroxide solution. Moreover, it is also possible to make embedding during metal wiring possible and to hold the property of outstanding self-flattening.
[0070] (Gestalt 3 of operation) Although the methyl system silane was used with the gestalten 1 and 2 of operation above, the same effect is done so even if it uses the monoethyl silane (SiH3 (C2H5)) which is an ethyl system silane, diethylsilane (SiH2(C2H5) 2), and a triethyl silane (SiH3 (C2H5)).
[0071] Hereafter, the gestalt 3 of implementation of this invention is explained based on drawing.
[0072] Drawing 9 is drawing showing typically the molecular structure at the time of forming a silicon oxide using a monoethyl silane. Drawing 10 is drawing showing typically the molecular structure at the time of forming a silicon oxide using diethylsilane. Drawing 11 is drawing showing typically the molecular structure at the time of forming a silicon oxide using a triethyl silane. Drawing 12 is a graph showing the specific inductive capacity of the silicon oxide of a Prior art, and the silicon oxide of the gestalt 3 of this operation.
[0073] The silicon oxide of the gestalt 3 of this operation manufactures a semiconductor device by the manufacture method shown by drawing 1 of the gestalt 1 of operation - drawing 3 like the HMO film 4 of the gestalt 1 of operation, and the silicon oxide 4 of the gestalt 2 of operation. Although the methyl system silane was used for a different point as a raw material, it is a point which is using the ethyl system silane. Moreover, the conditions (formation temperature, a formation pressure, quantity of gas flow, etc.) which form a silicon oxide in the gestalt 3 of this operation are the completely same conditions as the gestalten 1 and 2 of operation, and are performed by the plasma CVD method. It is the same as a monoethyl silane, diethylsilane, or a triethyl silane to create a silicon oxide according to the chemical reaction of the mixed gas which added only hydrogen peroxide solution, a silane, or hydrogen peroxide solution.
[0074] Hereafter, the reaction formula of the gestalt 3 of this operation is explained.
[0075] Intermediate field (C2H5) (OH) Si 3 and end-product Si(CH3) O1.5 are generated because the chemical reaction of the oxidation reaction (** 11) which shows a monoethyl silane below, and dehydration polymerization reaction (** 12) occurs.
[0076]
[Formula 11]

$$2\,SiH_3(C_2H_5) + 3\,H_2O_2 \rightarrow 2\,Si(C_2H_5)(OH)_3$$

[0077]
[Formula 12]

$$2\,n\,Si(C_2H_5)(OH)_3 \rightarrow 2\,n\,Si(CH_3)O_{1.5} + 3\,n\,H_2O$$

[0078] On the other hand, intermediate field (OH) Si 4 and an end product SiO2 are generated also for a silane because a chemical reaction (** 1, 2, 3, and 4) occurs. the intermediate fields of this Si (C2H5) (OH)3 and Si (OH)4, or Si (CH3) -- the silicon oxide 4 of drawing 3 is created by the chemical reaction of the end products of O1.5 and SiO2
[0079] Moreover, the silicon oxide 4 of drawing 3 is similarly formed because the chemical reaction of the oxidation reaction (** 13) which shows diethylsilane below, and dehydration polymerization reaction (** 14), and the chemical reaction (** 1, 2, 3, and 4) of a silane occur.
[0080]
[Formula 13]

$$SiH_2(C_2H_5)_2 + 2H_2O_2 \rightarrow Si(C_2H_5)_2(OH)_2$$

[0081]
[Formula 14]
$$n\ Si(C_2H_5)_2(OH)_2 \rightarrow n\ Si(C_2H_5)_2O_2 + n\ H_2O$$

[0082] In addition, about a triethyl silane, similarly, the silicon oxide 4 of drawing 3 is formed because the chemical reaction of oxidation reaction (** 15) and dehydration polymerization reaction (** 16) shown below and the chemical reaction (** 1, 2, 3, and 4) of a silane occur.
[0083]
[Formula 15]
$$SiH(C_2H_5)_3 + H_2O_2 \rightarrow Si(C_2H_5)_3(OH)$$

[0084]
[Formula 16]
$$n\ Si(C_2H_5)_3(OH) \rightarrow n\ Si(C_2H_5)_3O + n\ H_2O$$

[0085] Thus, since the silicon oxide 4 of drawing 3 generated from a monoethyl silane, diethylsilane, and the triethyl silane also holds the outstanding fluidity, embedding during aluminum wiring of microscopic ** is made possible.
[0086] The molecular structure of the silicon oxide of the gestalt 3 of this operation at the time of adding hydrogen peroxide solution and a silane to a monoethyl silane, diethylsilane, or a triethyl silane consists of Si-O combination, Si-OH combination, and Si-C2H5 combination, as shown in drawing 9 , drawing 10 , and drawing 11 . The rate of Si atom at this time for which it accounts in the silicon-oxide molecular structure as compared with Si atom of the HMO film 4 (drawing 4) of the gestalt 1 of operation and the silicon oxide 4 (drawing 6 , drawing 7) of the gestalt 2 of operation has decreased. For this reason, into the molecular structure, still more micro space will come to exist and the density of the whole silicon oxide will fall. Consequently, as for the silicon oxide 4 of the gestalt 3 of this operation, density will fall compared with the HMO film 4 of the gestalt 1 of operation, or the silicon oxide 4 of the gestalt 2 of operation. Of course, it could understand, even if that density is falling even if it compares with silicon-oxide 4p (drawing 18) of a Prior art doubles with the gestalten 1 and 2 of operation.
[0087] moreover, when it guesses from the experimental result of the gestalten 1 and 2 of operation, as it is shown in drawing 12 , to each specific inductive capacity of the silicon oxide of a Prior art and the silicon oxide of the gestalt 3 of this operation being the specific inductive capacity 4.5 of the silicon oxide by the Prior art, about 3.0 are expected and the silicon oxide by the gestalt 3 which is this operation is considered that decline in specific inductive capacity is achieved further
[0088] as explained above, even if it compares the specific inductive capacity of the silicon oxide by the gestalt 3 of this operation with the silicon oxide of a Prior art, or the silicon oxide of the gestalten 1 and 2 of operation, it becomes possible aiming at the fall which is specific inductive capacity]
[0089] Thus, the silicon oxide by invention of the gestalt 3 of this operation can acquire the effect of the reduction in a dielectric constant using the mixed gas of the mixed gas of a monoethyl silane, diethylsilane or a triethyl silane, a silane, and hydrogen peroxide solution or a monoethyl silane, diethylsilane or a triethyl silane, and hydrogen peroxide solution. Moreover, it is also possible to make embedding during metal wiring possible and to hold the property of outstanding self-flattening.
[0090] (Gestalt 4 of operation) Although the alkyl system silane was used with the gestalten 1, 2, and 3 of operation above, even if it uses a vinyl silane (SiH3 (CH=CH2)), the effect of a specific-inductive-capacity fall is similarly done so.
[0091] Hereafter, the gestalt 4 of implementation of this invention is explained based on drawing.
[0092] Drawing 13 is drawing showing typically the molecular structure at the time of forming a silicon oxide using a vinyl silane. Drawing 14 is a graph showing the specific inductive capacity of the silicon oxide of a Prior art, and the silicon oxide of the gestalt 4 of this operation.
[0093] In addition, the silicon oxide of the gestalt 4 of this operation manufactures a semiconductor device by the manufacture method shown by drawing 1 of the gestalt 1 of operation - drawing 3 like the HMO film 4 of the gestalt 1 of operation, and the silicon oxide 4 of the gestalten 2, 3, and 4 of operation. Although the alkyl silane was used for a different point in manufacture of the semiconductor device in this case as a raw material with the gestalten 1, 2, and 3 of operation, it is only having changed to the vinyl silane.
[0094] Moreover, the conditions (formation temperature, a formation pressure, quantity of gas flow, etc.) which form a silicon oxide in the gestalt 4 of this operation are the same conditions as the gestalten 1, 2, and 3 of operation, and the plasma CVD method is used for them. It is the same as a vinyl silane to create a silicon oxide according to the chemical reaction of the mixed gas which added only hydrogen peroxide solution, a silane, or hydrogen peroxide solution.
[0095] Hereafter, the reaction formula of the gestalt 4 of this operation is explained.
[0096] A vinyl silane is that the chemical reaction of oxidation reaction (** 17) and dehydration polymerization reaction (** 18) shown below occurs, and intermediate field (CH=CH2) (OH) Si 3 and an end product (CH=CH2) (OH) Si 3 are generated.
[0097]

[Formula 17]
$$2\,SiH_3(CH=CH_2)+3H_2O_2\rightarrow 2\,Si(CH=CH_2)(OH)_3$$

[0098]
[Formula 18]
$$2n\,Si(CH=CH_2)(OH)_3\rightarrow 2n\,Si(CH=CH_2)O_{1.5}+3nH_2O$$

[0099] On the other hand, intermediate field (OH) Si 4 and an end product SiO2 are generated also for a silane because a chemical reaction (** 1, 2, 3, and 4) occurs. The silicon oxide 4 of drawing 3 is formed of the chemical reaction of the end products of the intermediate fields of Si (CH=CH2) (OH)3 and Si (OH)4, and Si (CH=CH2) (OH)3, and SiO2.
[0100] In addition, since the silicon oxide 4 generated from the vinyl silane has the outstanding fluidity, it makes possible embedding during very detailed aluminum wiring.
[0101] The molecular structure of the silicon oxide 4 of the gestalt 4 of this operation at the time of adding hydrogen peroxide solution and a silane to a vinyl silane consists of Si-O combination, Si-OH combination, and Si-(CH=CH2) combination, as shown in drawing 13 . The rate of Si atom at this time for which it accounts in the silicon-oxide molecular structure as compared with Si atom of the HMO film 4 (drawing 4) of the gestalt 1 of operation and the silicon oxide (drawing 4 , drawing 6 , drawing 7 , drawing 9 , drawing 10 , drawing 11) of the gestalten 2 and 3 of operation has decreased. For this reason, into the molecular structure, still more micro space will come to exist and the density of the whole silicon oxide will fall. Consequently, as for the silicon oxide of the gestalt 4 of this operation, density will fall compared with the HMO film of the gestalt 1 of operation, and the silicon oxide of the gestalten 2 and 3 of operation. Of course, that density is falling could understand, even if it compares with silicon-oxide 4p (drawing 18) of a Prior art.
[0102] Thus, it becomes possible to aim at decline in specific inductive capacity because the density within the molecular structure of a silicon oxide falls. Moreover, it can bury by the silicon oxide 4 of the gestalt 4 of this operation of between the aluminum wiring 2, and it becomes possible to realize the outstanding self-flattening property.
[0103] as shown in drawing 14 which is the experimental result of the gestalt 4 of this operation, to each specific inductive capacity of the silicon oxide of a Prior art and the silicon oxide of the gestalt 4 of this operation being the specific inductive capacity 4.5 of the silicon oxide by the Prior art, the silicon oxide by the gestalt 4 of this operation is 2.7, and the fall which is specific inductive capacity much more further is achieved
[0104] as explained above, the specific inductive capacity of the silicon oxide by the gestalt 4 of this operation becomes possible [aiming at the fall which is specific inductive capacity] compared with the silicon oxide of a Prior art or the HMO film of the gestalt 1 of operation, and the silicon oxide of the gestalten 2 and 3 of operation
[0105] Thus, the silicon oxide by invention of the gestalt 4 of this operation can acquire the effect of the reduction in a dielectric constant using the mixed gas of a vinyl silane, a silane, and hydrogen peroxide solution, or the mixed gas of a vinyl silane and hydrogen peroxide solution. Moreover, it is also possible to make embedding during metal wiring possible and to hold the property of outstanding self-flattening.
[0106]
[Effect of the Invention] According to invention according to claim 1, it is effective in the ability of an embedding property to be able to offer the formation method of the silicon oxide which is well excellent in a self-flattening property low [a dielectric constant] by forming an insulator layer by the chemical-vapor-deposition method using the silane system gas containing the silicon atom combined with the silane system gas, the silane, the mixed gas of hydrogen peroxide solution, or the hydrocarbon group containing the silicon atom combined with the carbon hydrogen machine, and the mixed gas of hydrogen peroxide solution.
[0107] According to invention according to claim 2, also by the chemical-vapor-deposition method using the silane system gas combined with the alkyl group, a dielectric constant is low, and an embedding property is good, and it is effective in the ability to offer the formation method of the insulator layer which was excellent in the self-flattening property by making a hydrocarbon group into an alkyl group.
[0108] According to invention according to claim 3, it is effective in the ability of an embedding property to offer the formation method of the insulator layer which was well excellent in the self-flattening property low [a dielectric constant] also by the chemical-vapor-deposition method using the silane system gas combined with the methyl group, the dimethyl machine, or the trimethyl basis by making an alkyl group into a methyl group, a dimethyl machine, or a trimethyl basis.
[0109] According to invention according to claim 4, it is effective in the ability of an embedding property to offer the formation method of the insulator layer which was well excellent in the self-flattening property low [a dielectric constant] also by the chemical-vapor-deposition method method using the silane system gas combined with the ethyl group, the diethyl machine, or the triethyl machine by using an alkyl group as an ethyl group, a diethyl machine, or a triethyl machine.
[0110] According to invention according to claim 5, it is effective in the ability of an embedding property to offer the formation method of the insulator layer which was well excellent in the self-flattening property low [a dielectric constant] by making a hydrocarbon group into a vinyl group also by the chemical-vapor-deposition method using the silane system gas combined with the vinyl group.
[0111] According to invention according to claim 6, the range of the temperature at the time of insulator layer formation -10-60 degrees C, The range of the quantity of gas flow of 400 - 2000mTorr and a silane for the range of the pressure at the

time of insulator layer formation 0 - 120sccm, More ranges of the quantity of gas flow of the silane system gas containing the silicon atom combined with the hydrocarbon group than 0sccm by making the range of the quantity of gas flow of 120 or less sccms and hydrogen peroxide solution into 0.35 - 0.85 g/min It is effective in the ability of an embedding property to offer the formation method of the insulator layer which was well excellent in the self-flattening property low [a dielectric constant].
[0112] By the silicon atom which was equipped with the layer insulation film formed between multilayer metal wiring, and combined the layer insulation film with the hydrocarbon group being included a semiconductor substrate, the multilayer metal wiring formed on the semiconductor substrate, and on a semiconductor substrate according to invention according to claim 7 Since space is made in a layer insulation film, it is effective in the ability to offer the semiconductor device which has the insulator layer which it is low, the embedding property between ** and metal wiring is good, and the dielectric constant excelled in the self-flattening property.
[0113] According to invention according to claim 8, it is effective in the ability of the embedding property during metal wiring to offer the semiconductor device which has the insulator layer which was well excellent in the self-flattening property low [a dielectric constant] by forming a layer insulation film by the insulator layer formation method of a semiconductor device according to claim 1 to 6.
[0114] The 1st process for which a semiconductor substrate is prepared according to invention according to claim 9, By having the 2nd process which forms metal wiring on a semiconductor substrate, and the 3rd process which forms a wrap insulator layer for the metal wiring on a semiconductor substrate, and forming an insulator layer in a claim 1 or 6 by the insulator layer formation method of the semiconductor device a publication at either It is effective in the ability of the embedding property during metal wiring to offer the manufacture method of a semiconductor device of having the insulator layer which was well excellent in the self-flattening property, low [a dielectric constant].

[Translation done.]

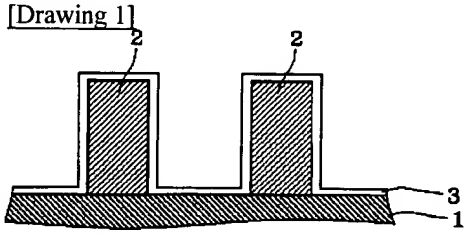
DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the cross section showing typically the manufacturing process of the layer insulation film by the gestalten 1-3 of implementation of this invention.
[Drawing 2] It is the cross section showing typically the manufacturing process of the layer insulation film by the gestalten 1-3 of implementation of this invention.
[Drawing 3] It is the cross section showing typically the manufacturing process of the layer insulation film by the gestalten 1-3 of implementation of this invention.
[Drawing 4] It is drawing having shown typically the molecular structure of the silicon oxide by the gestalt 1 of implementation of this invention.
[Drawing 5] It is the graph which showed the measurement result of the specific inductive capacity of the silicon oxide by the gestalt 1 of implementation of this invention, and the specific inductive capacity of the silicon oxide of a Prior art.
[Drawing 6] It is drawing having shown typically the molecular structure of the silicon oxide by the gestalt 2 of implementation of this invention.
[Drawing 7] It is drawing having shown typically the molecular structure of the silicon oxide by the gestalt 2 of implementation of this invention.
[Drawing 8] It is the graph which showed the measurement result of the specific inductive capacity of the silicon oxide by the gestalt 2 of implementation of this invention, and the specific inductive capacity of the silicon oxide of a Prior art.
[Drawing 9] It is drawing having shown typically the molecular structure of the silicon oxide by the gestalt 3 of implementation of this invention.
[Drawing 10] It is drawing having shown typically the molecular structure of the silicon oxide by the gestalt 3 of implementation of this invention.
[Drawing 11] It is drawing having shown typically the molecular structure of the silicon oxide by the gestalt 3 of implementation of this invention.
[Drawing 12] It is the graph which showed the prospective value of the specific inductive capacity of the silicon oxide by the gestalt 3 of implementation of this invention, and the measurement result of the specific inductive capacity of the silicon oxide of a Prior art.
[Drawing 13] It is drawing having shown typically the molecular structure of the silicon oxide by the gestalt 4 of implementation of this invention.
[Drawing 14] It is the graph which showed the measurement result of the specific inductive capacity of the silicon oxide by the gestalt 4 of implementation of this invention, and the specific inductive capacity of the silicon oxide of a Prior art.
[Drawing 15] It is the cross section showing the manufacturing process of the conventional layer insulation film typically.
[Drawing 16] It is the cross section showing the manufacturing process of the conventional layer insulation film typically.
[Drawing 17] It is the cross section showing the manufacturing process of the conventional layer insulation film typically.
[Drawing 18] It is drawing having shown the molecular structure of the conventional silicon oxide typically.
[Description of Notations]
1 A silicon substrate, 2 3 Aluminum wiring, 5 A plasma oxidation film, 4 A silicon oxide, 6 Layer insulation film.

[Translation done.]

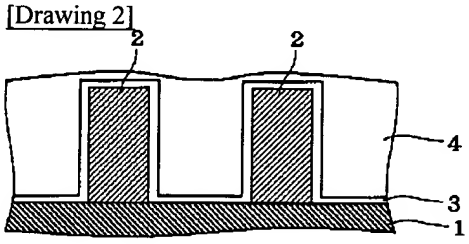
DRAWINGS

[Drawing 1]



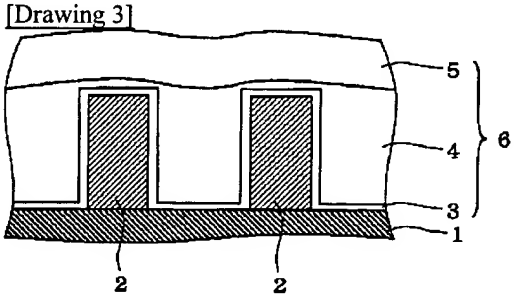
1：シリコン基板
2：アルミ配線
3：プラズマ酸化膜

[Drawing 2]



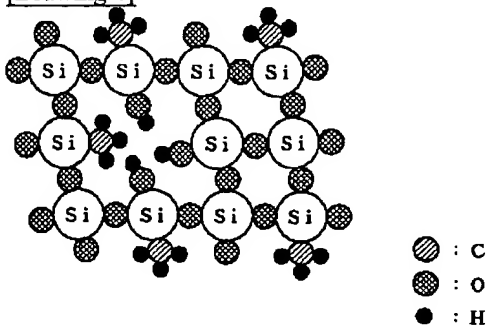
4：シリコン酸化膜(ＨＭＯ膜)

[Drawing 3]

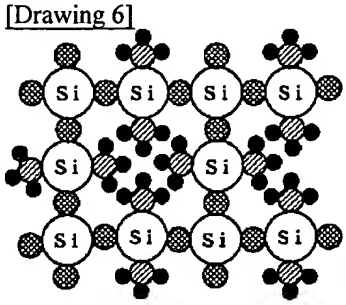


5：プラズマ酸化膜
6：層間絶縁膜

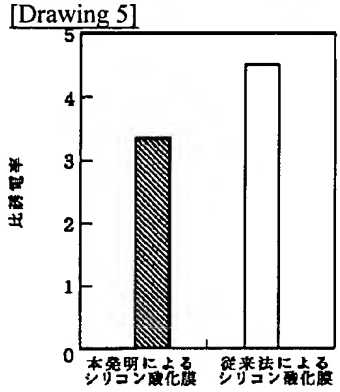
[Drawing 4]



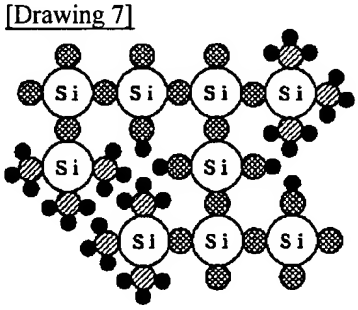
[Drawing 6]



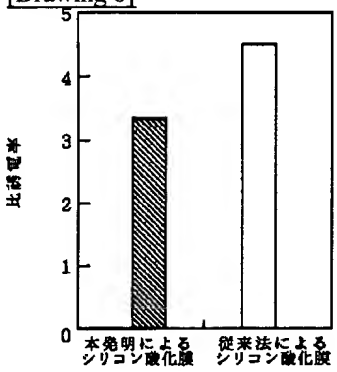
[Drawing 5]



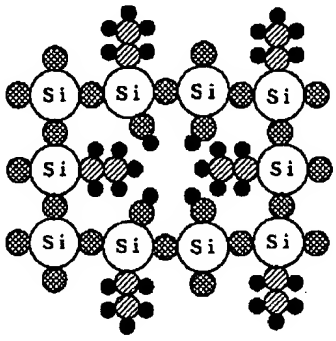
[Drawing 7]



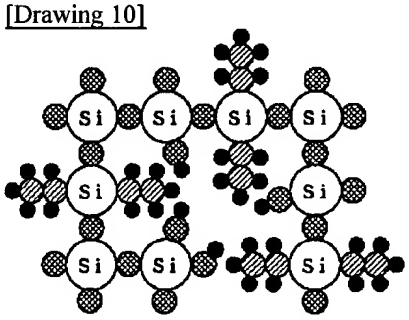
[Drawing 8]



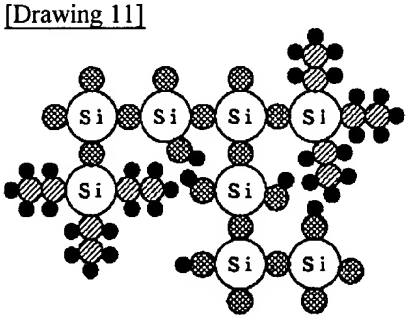
[Drawing 9]



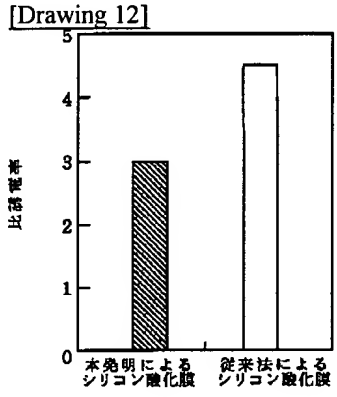
[Drawing 10]



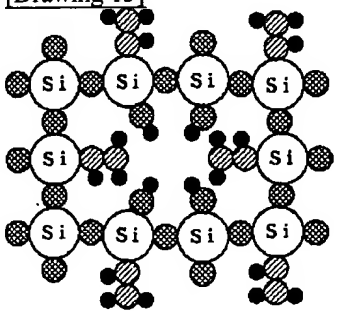
[Drawing 11]



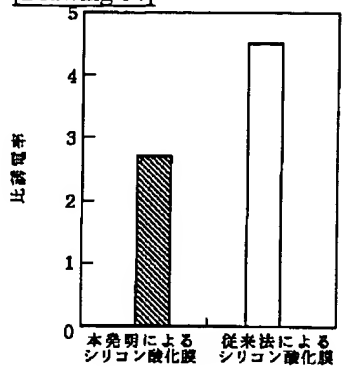
[Drawing 12]



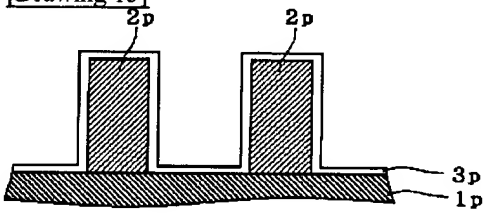
[Drawing 13]



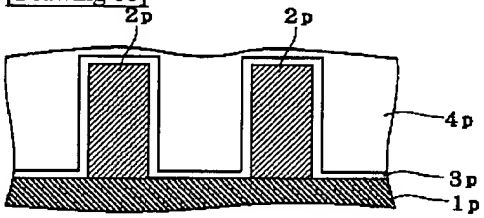
[Drawing 14]



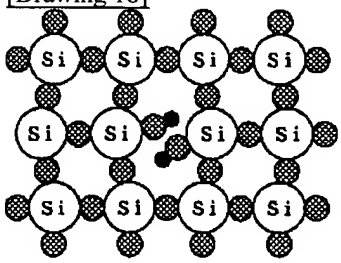
[Drawing 15]



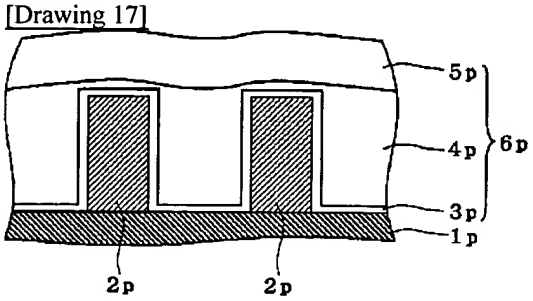
[Drawing 16]



[Drawing 18]



[Drawing 17]



[Translation done.]